REMARKS

In response to the Final Official Action mailed October 22, 2003, Applicants respectfully request that the Examiner reconsider the rejection of the remaining claims.

Claims 1-6, 8 and 10-20 remain in this application.

Claims 1, 4-6 and 8 are being amended.

The Examiner has rejected Claims 1-2, 4-6, 8 and 10-20 under 35 U.S.C. 102(b) as being anticipated by *McGrath*, et al. (U.S. Patent No. 5,345,409) (hereinafter "the *McGrath* reference). Applicants respectfully traverse these rejections.

In the Final Office Action issued in the parent case, the Examiner submitted that the *McGrath* reference teaches a program - configurable delta – sigma modulator in Figures 1,3, and 7, and in the text at Col. 19, Lines 8 – 13, Col. 6, Line 55, Col. 17, Lines 51 – 52, Col. 22, Lines 2 – 4, and Tables 2 and 5. This is clearly incorrect, as none of these citations, either alone or in combination, discloses a delta sigma modulator with a program – configurable topology, and in particular a delta-sigma modulator having a topology including a set of configurable arithmetic and logic blocks.

Specifically, Figure 1 of the *McGrath* reference only shows a set of simple blocks 120 generally representing a corresponding set of delta – sigma modulators. The particular topology and order of these modulators is not shown. Similarly, Figures 3 and 7 only teach a signal processor and its associated memory maps, and nowhere shows a delta – sigma modulator of any topology or order.

None of the textual excerpts cited at Col. 19, Lines 8 – 13, Col. 6, Line 55, Col. 17, Lines 51 – 51, Col. 22, Lines 2 – 4, and Tables 2 and 5, teach that delta – sigma modulators 120 of Figure 1 are programmable, and particularly that the topology of those delta –sigma modulators is configurable in programming.

Specifically, the textual excerpt at Col. 19, Lines 8 – 13 of the *McGrath* reference, merely discusses the general programmability of digital signal processing operations of device 10 shown in Figure 1. The excerpt at Col. 6, Line 55, makes a general statement that adaptive processing can be implemented using programming. The excerpt at Col. 17, Lines 51 – 51,

describes cycling of decimated data in a cyclical register. Finally, the excerpt at Col. 22, Lines 2 – 4, of the *McGrath* reference discusses the generation of discrete Fourier transforms (DFTs), and not the programmability of delta – sigma modulators or delta – sigma algorithms. Tables 2 – 5 show a general set of digital signal processor instructions, rather than specific instructions for programming a delta – sigma modulator.

The Examiner also submitted that the *McGrath* reference discloses, at Figures 1 – 15, and Col. 21, Line 55 et seq., a multiple order delta – sigma algorithm. This is also incorrect. The McGrath reference describes infinite impulse response (IIR) algorithms and DCT algorithms, but not delta –sigma modulation algorithms, of any type.

The *McGrath* reference discloses adders, multipliers, shifters and pipelining; however, none of these structures and / or functions forms a part of a program configurable delta – sigma modulator. For example, Figure 5 illustrates a multiplier – accumulate processor and Figure 12 shows a general digital signal processor system.

The Examiner has also rejected Claims 1-2, 4-6, 8 and 10-12 under 35 U.S.C. 102(b) as being anticipated by *Knudsen* (U.S. Patent No. 5,781,137) (hereinafter "the *Knudsen* reference). Applicants also traverse these rejections.

Specifically, the Examiner submitted that the *Knudsen* reference teaches in the Abstract, Summary, and block 100, a delta –sigma modulator with a configurable topology. Applicants respectfully disagree.

Figure 8 of the *Knudsen* reference illustrates a data converter 82 having an output coupled to a programmable digital analyzer 100. The output of the programmable digital analyzer 100 is then utilized in digital correction block 84 for reducing linearity errors, as described in the Abstract and Summary cited by the Examiner.

Programmable digital analyzer 100 does not change the topology of delta –sigma modulator 82, and only operates on the output signal from delta –sigma modulator 82, through digital correction circuitry 84. The topology and order of delta –sigma modulator 82 is fixed.

The Examiner has also rejected Claim 5 under 35 U.S.C. 102(b) as being anticipated by *Norsworthy* (U.S. Patent No. 5,420,584) (hereinafter "the *Norsworthy* reference). Applicants respectfully traverse this rejection.

Specifically, the Examiner additionally submitted in the Final Office Action in the parent case that the *Norsworthy* reference discloses a delta – sigma modulator configurable in response to a selected program to a selected data rate. The Examiner cites the Abstract, Summary, and Figures 1 –3. The Examiner's submissions with respects to the *Norsworthy* reference are, however, also clearly incorrect.

The *Norsworthy* reference discloses, in Figures 1 – 3, a data converter that includes delta –sigma modulators 18 and 716 in corresponding signal paths including barrel shifter selectors 80 and 34. As precisely described in the Abstract, the barrel shifter selectors change the bit width of the data being transmitted through each of the bit paths.

The *Norsworthy* reference provides little description of delta-sigma modulators 18 and 716, and in particular, only provides generalized blocks representations of modulators 18 and 716 in Figure 1. In any event, there is no teaching in the *Norsworthy* reference that delta- sigma modulators 18 and 716 are themselves programmable, and specifically programmable to that data rate. It appears that the topologies of these delta – sigma modulators are fixed.

The Patent Examiner has also rejected Claim 3 under 35 U.S.C. 103(a) as being unpatentable over the *McGrath* reference and/or the *Knudsen* reference in view of *Keevill, et al.* (U.S. Patent No. 6,359,938) (hereinafter "the *Keevill* reference") and/or the *Norsworthy* reference. Applicants also respectfully traverse these rejections.

The *Keevill* reference discloses a sigma delta modulator in Figure 17 but only briefly mentions the characteristics of this delta sigma modulator at Col. 19, Lines 24 - 31. The *Keevill* reference does not describe the delta – sigma modulator of Figure 17 as programmable; the topology appears to be fixed.

No new matter has been added; Applicants have merely amended the claims to further clarify the invention disclosed in these claims. Applicants respectfully submit that the claims as they now stand are patentably distinct over the art cited.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 745-5374.

Respectfully submitted,
WINSTEAD SECHREST & MINICK P.C.
Attorneys for Applicants

Date: 3-12-04

By: James J. Murphy
James J. Murphy
Reg. No. 34,503

P. O. Box 50784
Dallas, Texas 75201
(214) 745-5374

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